

<p>Substitute for form 1449A/PTO</p> <p><b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b></p> <p>(use as many sheets as necessary)</p> <p>1 Sheet 1 of 1</p>				<p><b>Complete if Known</b></p> <table border="1"> <tr> <td><b>Application Number</b></td> <td>10/040,940</td> </tr> <tr> <td><b>Filing Date</b></td> <td>January 9, 2002</td> </tr> <tr> <td><b>First Named Inventor</b></td> <td>Allon ADIR et al</td> </tr> <tr> <td><b>Group Art Unit</b></td> <td>2857</td> </tr> <tr> <td><b>Examiner Name</b></td> <td></td> </tr> <tr> <td><b>Attorney Docket Number</b></td> <td>ADIR=1</td> </tr> </table>		<b>Application Number</b>	10/040,940	<b>Filing Date</b>	January 9, 2002	<b>First Named Inventor</b>	Allon ADIR et al	<b>Group Art Unit</b>	2857	<b>Examiner Name</b>		<b>Attorney Docket Number</b>	ADIR=1
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
XS	AC	A. CHANDRA, et al "AVGEN - A Test Generator for Architecture Verification" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol. 3, No. 2, pp. 188-200, June 1995.	
XS	AD	Yossi LICHTENSTEIN et al, "Model Based Test Generation for Processor Verification" IBM Israel Science and Technology, Sixth Innovative Applications of Artificial Intelligence Conference, August 1994, pp. 83-94.	

Examiner Signature	Tingting Sun	Date Considered	02/06/04
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